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Order Number

Serial Number

PRODUCT TEST MANUAL

2SY110K28 SYNCHRONISM CHECK RELAY

lssue Level	Date	Summary of changes
D	12/12/1996	Initial issue.

Due to RMS continuous product improvement policy this information is subject to change without notice.

Document updated	Checked	Registered	.pdf file created	.pdf uploaded to web site



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1. BRIEF DESCRIPTION

The 2SY110 synchronism check relay is designed to measure the phase angle between the monitored single phase voltages on the line & bus sides of a breaker & verify this angle is less than or equal to the front panel setting. If the measured angle has met this criteria for the time period defined by the front panel setting & the voltage magnitudes are both above a minimum level for normal operation or below a reduced minimum level for dead line or dead bus operation, the output relay is energised & the breaker will be permitted to close. Resetting will occur if phase angle or either voltage magnitude strays outside the limits. A panel mounted LED provides visual indication of a sync. check function in progress.

2. SPECIFICATION

PHASE ANGLE

Setting:

Setting :

Setting:

20-100 degrees continuously adjustable over a linear scale +2% +2.5 degrees

DELAY TIMER Setting range:

Repeatability :

Repeatability :

1 to 10 seconds +2% +0.5 second

SENSING VOLTAGE

63.5 volt 50Hz

BURDENS

Sensing voltage : 1.5VA Auxiliary supply : 10W (110V DC unit)

DEAD LINE & DEAD BUS SELECTION

Selection is by means of internal control relays wired to the rear terminals .

DEAD LINE & DEAD BUS SELECTION THRESHOLD

This is factory preset at 15% nominal sensing voltage +/-1.5%.

OPERATION INDICATION

The relay is fitted with a LED indicator to show synchronism check is in progress.

UNDERVOLTAGE LOCKOUT

This is factory preset at nominally 80% of nominal input & is set to within approximately +/-1.5% of nominal. Selection of "dead" or "minimum" line or bus overrides the undervoltage lockout.

INSULATION WITHSTAND

In accordance with AS2481-1981 (clause 5-4), IEC 255-5:

2KV RMS between input & frame, output & frame, & output & input. 1.2/50 5KV impulse between each terminal & earth, between circuits not normally connected together & between terminals of the same circuit.

NOISE IMMUNITY

Withstands the high frequency interference test detailed in AS2481-1981 (clause 5-5 App. D), IEC 255-22-1.

OUTPUT CONTACTS

The output relay is fitted with 2 changeover self reset fine silver contacts as standard. Magnetic blowouts are fitted to increase contact switching performance.

2. SPECIFICATION (Cont)



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30R RELAY CONTACT RATINGS (Time delayed contacts)

Make & Carry Continuously

3,000 VA AC resistive with maximums of 660V & 12A 3,000 VA DC resistive with maximums of 660V & 12A

Make & Carry for 0.5 Seconds

7,500 VA AC resistive with maximums of 660V & 30A 7,500 VA DC resistive with maximums of 660V & 30A

AC Break Capacity

3,000 VA AC resistive with maximums of 660V & 12A

DC Break Capacity (Amps)

Voltage	24	48	125	250		
Resistive Rating	а	12	1.5	0.5	0.25	
C			12	12	10	5
	Max Break	а	12	1	0.4	0.2
L/R 40 mS		b	30	15	5.5	3.5
	N3 Rating					
	1000 Ops	b	12	12	5	2.5

a = Without magnetic blowouts b = With magnetic blowouts

* As tested by Powernet Yarraville laboratories in Victoria.

3. TEST EQUIPMENT REQUIRED

2 x AC 0-300 Amplifiers 50 Hz Oscillator 50 Hz Adjustable Phase Shifter Digital Voltmeter Oscilloscope, Dual Trace Frequency Counter PU/DO Measuring Instrument Decade Boxes High Voltage Test Equipment

4. ASSOCIATED DRAWINGS

660-116-206Circuit Diagram, PCB Phase Angle Measuring660-116-306Loading diagram, PCB Phase Angle Measuring660-128-201Circuit diagram, PCB Quad Voltage Sensing and Tim660-128-201Loading diagram, PCB Quad Voltage Sensing and Tim	171-110-128	2SY110K28 Wiring Diagram
660-116-306Loading diagram, PCB Phase Angle Measuring660-128-201Circuit diagram, PCB Quad Voltage Sensing and Tim660-128-201Loading diagram PCB Quad Voltage Sensing and tim	660-116-206	Circuit Diagram, PCB Phase Angle Measuring
660-128-201 Circuit diagram, PCB Quad Voltage Sensing and Tin	660-116-306	Loading diagram, PCB Phase Angle Measuring
660 129 201 Looding diagram DCP Qued Voltage Sensing and tin	660-128-201	Circuit diagram, PCB Quad Voltage Sensing and Timer
Loading diagram, PCB Quad voltage Sensing and tim	660-128-301	Loading diagram, PCB Quad Voltage Sensing and timer

5. HIGH VOLTAGE TESTING

- a) Apply 2KV RMS 50Hz between all terminals tied together and frame for one minute.
- b) Apply 3 5KV 1/50us impulses of each polarity between all terminals tied together and frame.



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6. CALIBRATION & TEST PROCEDURE

6.1 General

The phase angle measuring circuitry in this unit is fed from a low voltage (10 volt nominal) winding on each of the two input interfacing transformers. The two input signals are fed into separate squaring amplifiers and the output square waves mixed to generate a rectangular wave with the negative going pulse length proportional to the incoming phase angle difference. This waveform controls the up integration time of a linear integrator and when the negative going pulse has passed, the integrator resets to zero, ready for the next pulse. The resultant output waveform is triangular with a rising edge and exponentially decaying trailing edge. The amplitude is proportional to the phase difference between the AC input signals. A front panel variable threshold level detector is used to sense if the height of this waveform exceeds a pre-set value (representing the phase angle setting). The resultant output is pulses edge clock a 3 stage binary counter to give a continuous "out of phase" signal if this condition exists. A second binary counter (4 stage) is clocked by the integrator control waveform and is reset by any "out of phase" pulses. If this counter times out it resets the 3 stage counter, thus signalling the "in phase" condition.

The voltage sensing circuitry used on the 660/128 - 1 PCB contains two identical "perfect rectifier" and smoothing circuits each fed from a 10 volt transformer secondary winding. The DC outputs are each fed into two separate comparators to give a logic level corresponding to the following,

V Bus > 80% V Line > 80% V Bus > 15% V line > 15%

These signals are fed via combinational logic on the 660/128 - 3 PCB back to the timer initiate input on the 660/116-5 PCB.

The timer on the voltage measuring board is initiated from the above mentioned circuitry and contains a front panel variable oscillator and ripple counter to give a continuous output "high" when the count reaches 8192.

6.2. Calibration of 660/128-1 Voltage Sensing Circuit

- a) Component reference number refer to circuit diagram 660-128-201.
- b) Cut links A, B & C on the MC14541 to set the count to 8192.
- c) Apply 50 Volt auxiliary supply between terminals 1 (positive) and 3 (negative).
- d) Apply 50 Volts DC to the Dead line (terminals 19 & 20) and Dead Bus (terminals 21 & 22) relays.
- e) Apply AC amplitude and phase variable supplies to the unit as per QEC Drawing A1-H-111788-06.
- f) Set Bus input to 50.5 volts and adjust trimpot ("B80") until PCB pin 23 just goes high at this input voltage. (V Bus > 80%).

Minimum	Nominal	Maximum	Actual	Units
49.5	50.5	51.5		Volts



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g) Set Bus input to 9.5 volts and adjust trimpot R27 ("B15") until PCB pin 22 just goes high at this input voltage. (V Bus < 15%).

Minimum	Nominal	Maximum	Actual	Units
8.5	9.5	10.5		Volts

Set line input to 50.5 volts and adjust R29 ("L80") until PCB pin 13 just goes high at this input voltage. (V Line > 80%).

Minimum	Nominal	Maximum	Actual	Units
49.50.	50.5	51.5		Volts

i) Set Line input to 9.5 volts and adjust trimpot R31 ("L15") until PCB pin 12 just goes high at this input voltage. (V Line < 15%).

Minimum	Nominal	Maximum	Actual	Units
8.5	9.5	10.5		Volts

6.3 Calibration of 660/128-1 Timer

- a) Initiate timer by making taking PCB pin 8 to zero volts (connect pin 17 to pin 8).
- b) Adjust trimpot R18 to give a scale ends minimum ratio of 10 : 1 as measured at PCB pin 11 irrespective of actual values.
- c) Check the following accuracy initiating the timer via pin 8. Note that waveform period at PCB pin 11 at maximum time setting is approximately 2.441 ms.

Minimum	Nominal	Maximum	Actual	Unit
.7	1	1.3		Seconds
3.7	4.0	4.3		
6.7	7.0	7.3		
9.7	10.0	10.3		

6.4 Calibration of 660/116-6 Phase Angle Circuitry

- a) Component reference numbers refer to circuit diagram 660-116-6.
- b) Apply 63.5 volts 50 Hz to Bus and Line inputs. Set phase difference to zero. Measure by using a Dual Beam Oscilloscope or Phase Angle meter.
- c) Check that IC1 pin 8 is high. If a small phase difference is exists between the Bus
- and

6.4

Line inputs a small negative going pulse of width equal to the phase difference will appear at pin 8. If either of the input transformers is incorrectly wired IC1 pin 8 waveform will be a square wave for the "in phase" condition.

- d) Set trimpot to R22 to the middle of its range, and the dial setting pot to 100⁰.
- d) Set incoming phase angle to 100[°], and adjust trimpot R15 until PCB pin 6 just goes high (in phase condition).
- f) Set incoming phase angle to and dial setting pot to 20° .
- g) Adjust R22 until PCB pin 6 just goes high.

Calibration of 660/116-6 Phase Angle Circuitry (Cont)

h) Repeat the above steps until the dial scale is calibrated.



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i) Check setting accuracy as per table below.

Minimum	Nominal	Maximum	Actual	Unit
16	20	24		Degrees
36	40	44		
56	60	64		
76	80	84		
96	100	104		

7. GENERAL & FUNCTIONAL

a) Check for correct operation of the timer logic by observing that PCB pin 8 (motherboard avlug L1) goes low in the following cases.

b) Bus voltage greater than 50.5 volts and line voltage greater that 50.5 volts and inputs

"in phase".

- b) Bus voltage greater than 50.5 volts and line voltage less than 9.5 volts and Dead Line select relay energised.
- c) Line voltage greater than 50.5 volts, bus voltage less than 9.5 volts and Dead Bus select relay energised.
- e) Bus and Line voltages at 30 volts, Min. Bus and Min. Line switches "in" and inputs in phase.
- f) Check that the relay is electrically sound and mechanically robust as per Standard Inspection & Test Schedule 903-000-026.

PASS

TESTED BY :_____DATE :_____



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8.0 CONNECTION DIAGRAM



